

Fig. 1 (Prior Art)

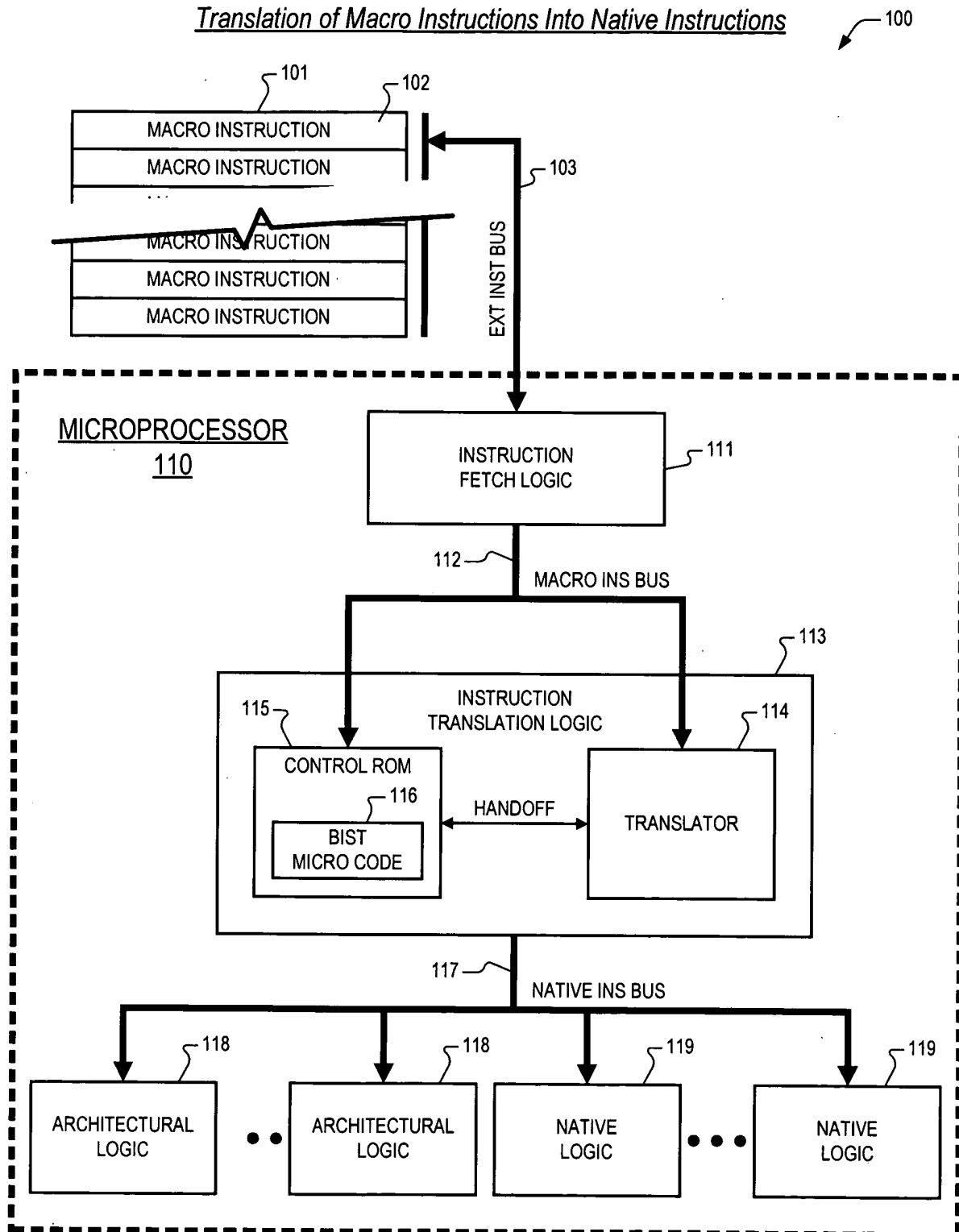
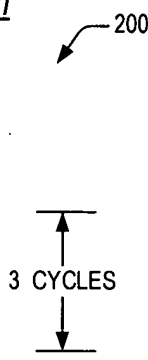


Fig. 2

Indirect Specification of Native Register via Macro Instruction

CYCLE	MACRO INS BUS	NATIVE INS BUS
1	ADD [EAX],FFFFFFFh	+++
2	***	LD NR1,[EAX]
3	***	ADD NR1,NR1,FFFFFFFh
4	***	ST [EAX],NR1

Fig. 3

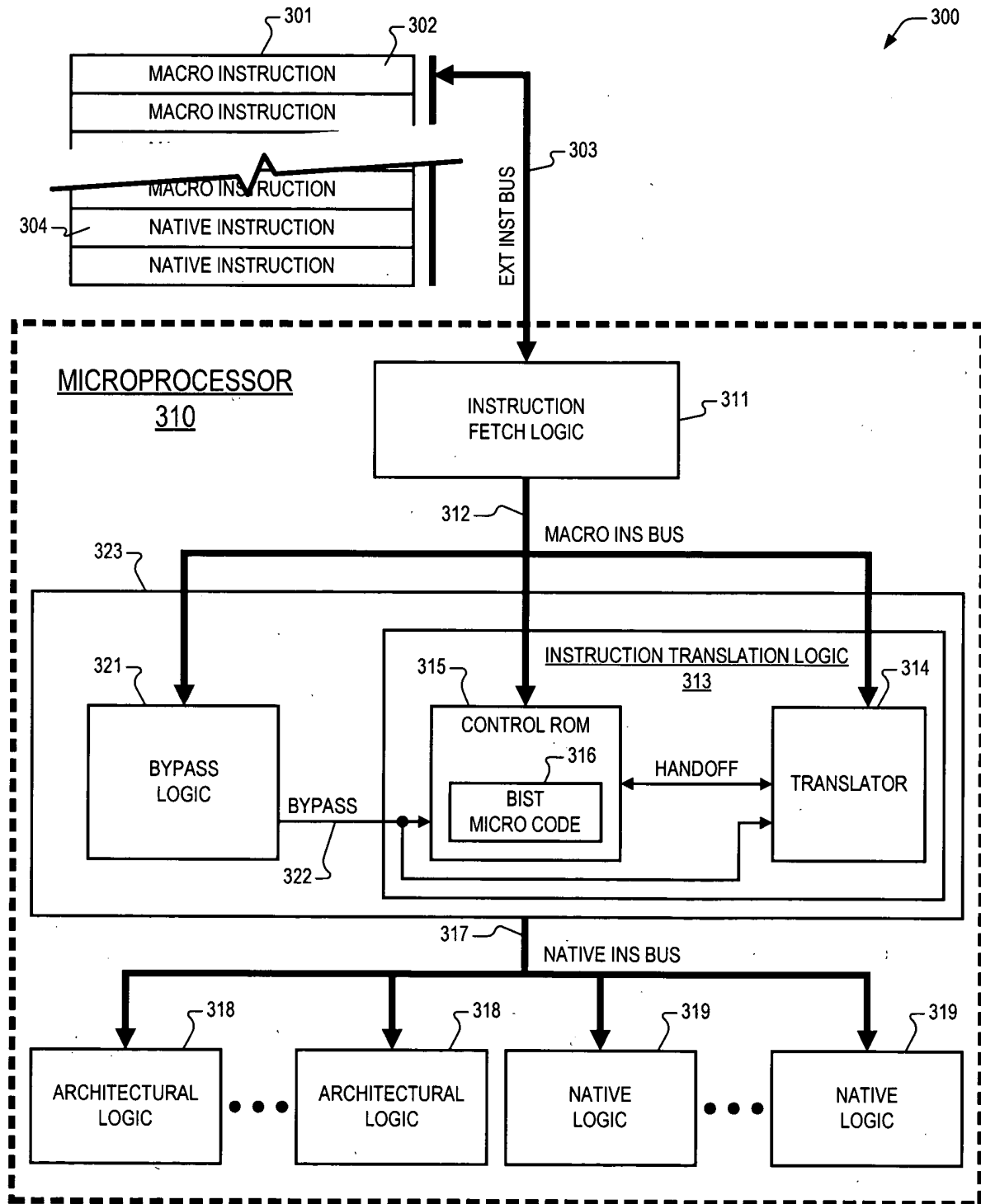
Translator Bypass for Native Instructions

Fig. 4

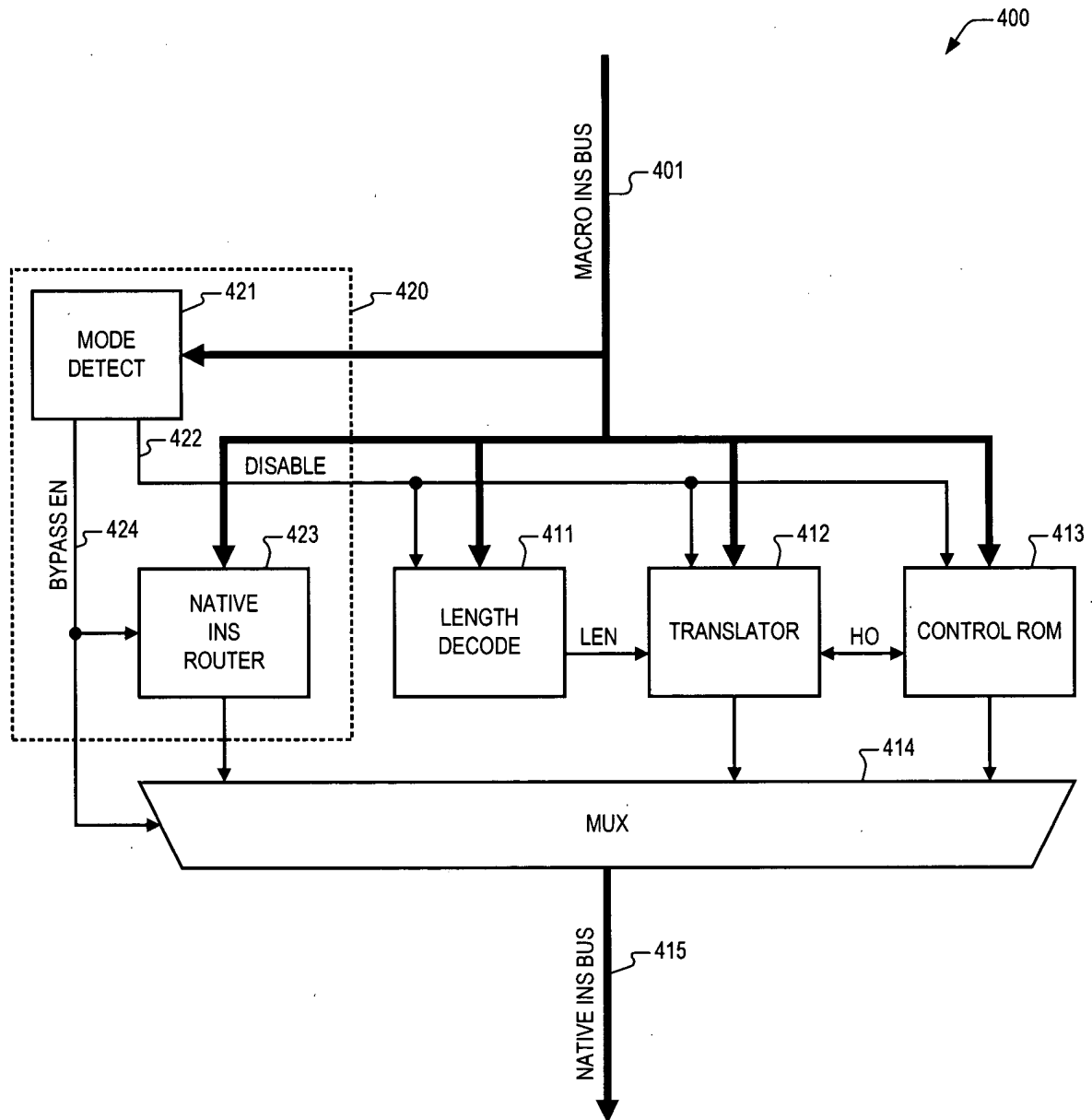
Translate Stage Logic for Native Instruction Bypass Mode

Fig. 5

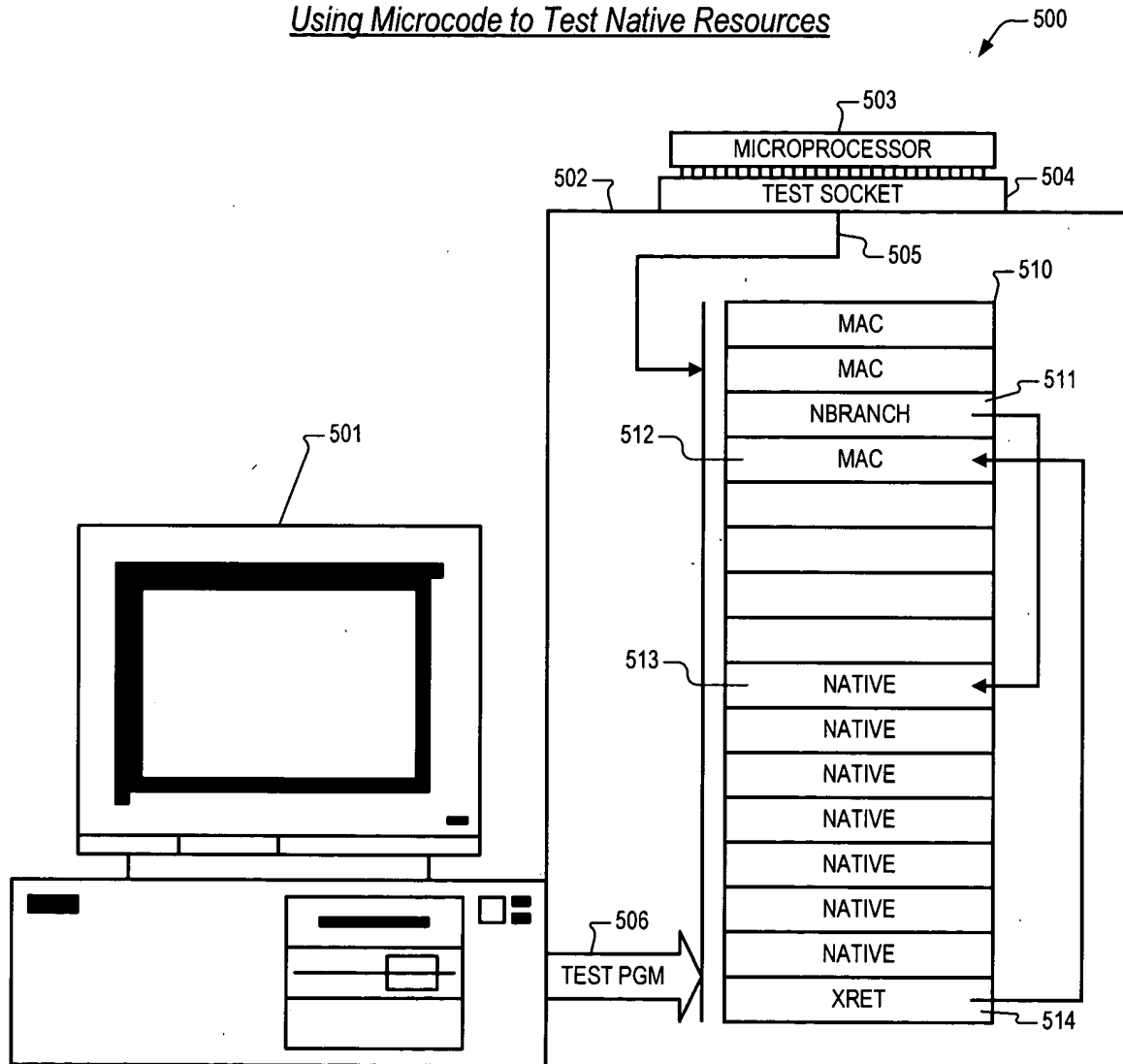
Using Microcode to Test Native Resources

Fig. 6

Instruction Sequence for Testing Native Registers

600

CYCLE	MACRO INS BUS	NATIVE INS BUS
1	MOV EAX,TST1	+++
2	MOV EBX,OUTBFR	LD EAX,TST1
3	NBRANCH	LD EBX,OUTBFR
4	LD T1,0	JMP [EAX]
5	ST [EBX],T1	LD T1,0
6	NOT T1	ST [EBX],T1
7	ST [EBX],T1	NOT T1
8	***	ST [EBX],T1
9	***	

		+++
1001	XRET	+++
1002	NEXT MAC	JMP [EAX+1]
1003	***	NEXT MAC

Fig. 7

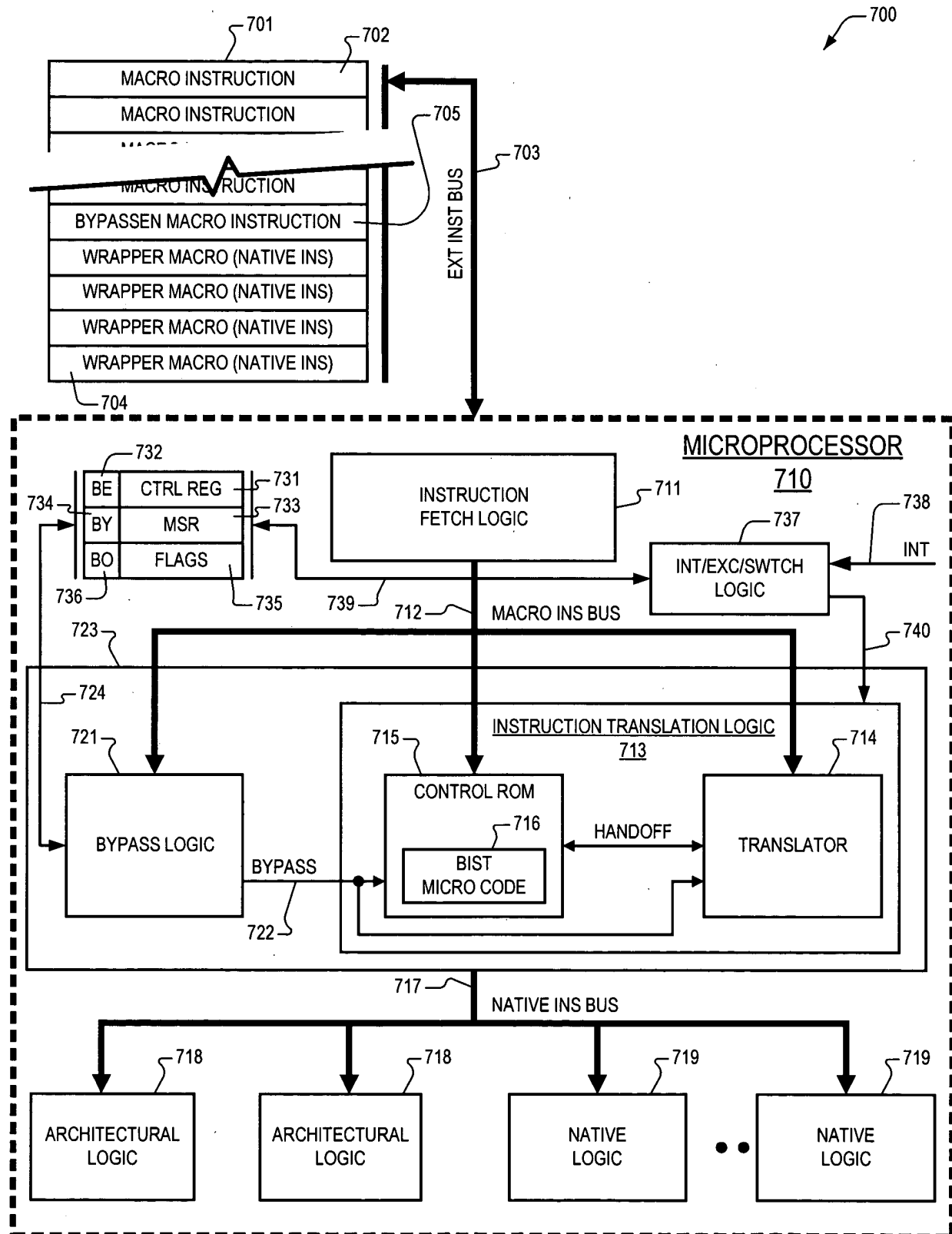
Microprocessor for Executing Native Applications

Fig. 8

Interrupt-Transparent Native Application Instruction Sequence